Product : Nemeus – XM001

Doc : Specifications

Reference : Spec_XM001_v1.0

History : V1.0

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History

Version	Date	Author	Comments
V1.0	17/10/2017	Isabelle Tocquer	Initial

Purpose

This document describes the XM001 V1.2 product specification for EU and Japan markets. The product is compatible to XBEE size and connexion format.

Overview

The main characteristics of the product are:

For EU area:

- LoRa™ WAN 1.0.2 EU Class A & C
    - Activation by Personalization (ABP)
    - Over-The-Air Activation (OTAA)
- SIGFOX™ ready
- Fully certified on major LoraWan & Sigfox networks
- Easy to use and deploy
- External power supply 3V/80mA
- RoHS conform / Pre-Certified ETSI EN 300-220 / RED compliance

For Japan market:

- LoRa™ WAN 1.0.2 JP Class A & C
    - Activation by Personalization (ABP)
    - Over-The-Air Activation (OTAA)
- SIGFOX™ ready (certification ongoing)
- Easy to use and deploy
- External power supply 3V/80mA
- RoHS conform / MIC compliant under number R018-160290 for LORA modulation

RF performances

- Frequency bands:
    - For EU: 863-870MHz
    - For Japan:
        - 920.6 to 928MHz (BW=200kHz, G1D, 100kHz separation, 74 channels)
        - 920.7 to 927.9MHz (BM=400kHz, G1D, 100kHz separation, 72 channels)
- TX Power = 14dBm (25 mW) for EU market
- TX Power = 13dBm for Japan market
- RX Sensitivity -137dBm in LORA mode, SF=12
- Approx. 10 km range
- External antenna connexion: via SMA or UFL connectors

Electricals characteristics

Power efficient:

- IDLE : < 2uA
- Tx mode : 39,5mA (for LoRa™) to 50mA (for SigFox™)
- Rx mode : 11,7mA

Supply:

- Minimum voltage= 2.7V
- Recommended voltage=3V
- Maximum voltage= 3.3V

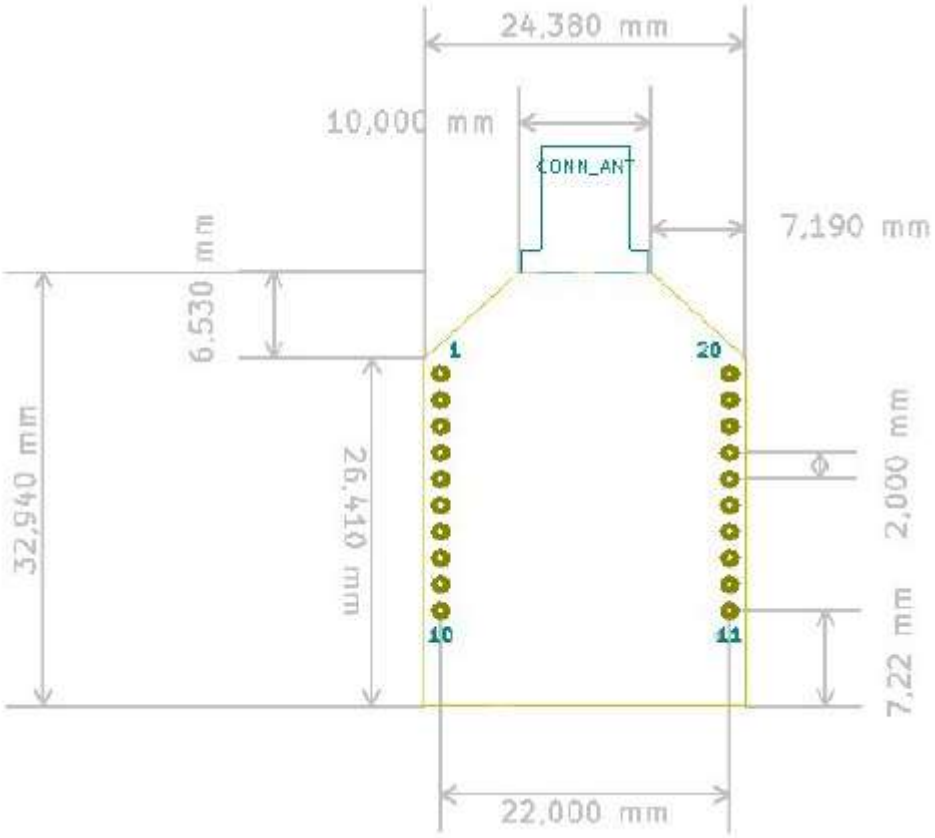
Environment

Operating temperature -30°C to +85°C

Storage temperature -40°C to 85°C

Mechanics

The product is conformed to XBEE mechanical standards.

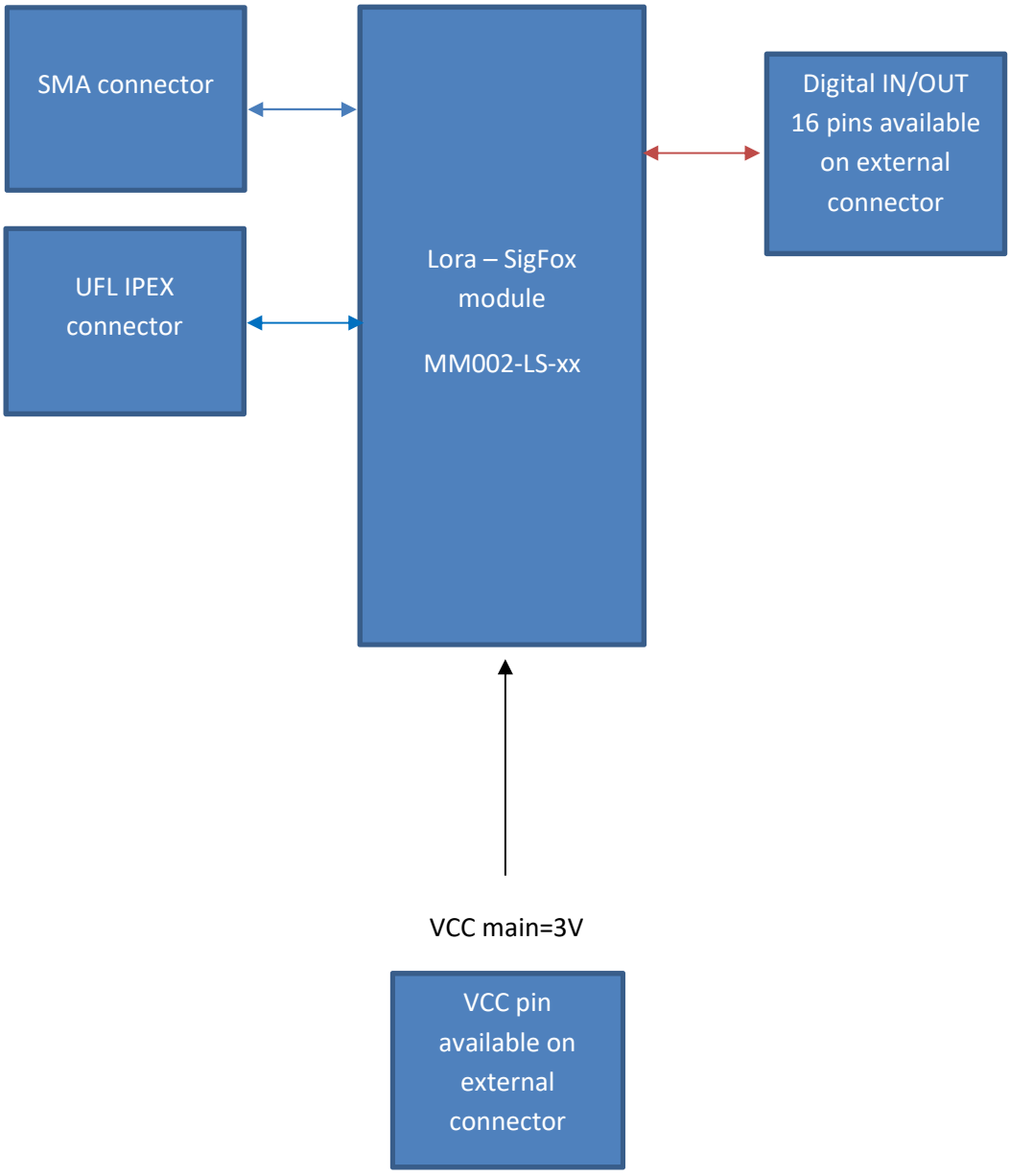


PCB thickness=1.6mm

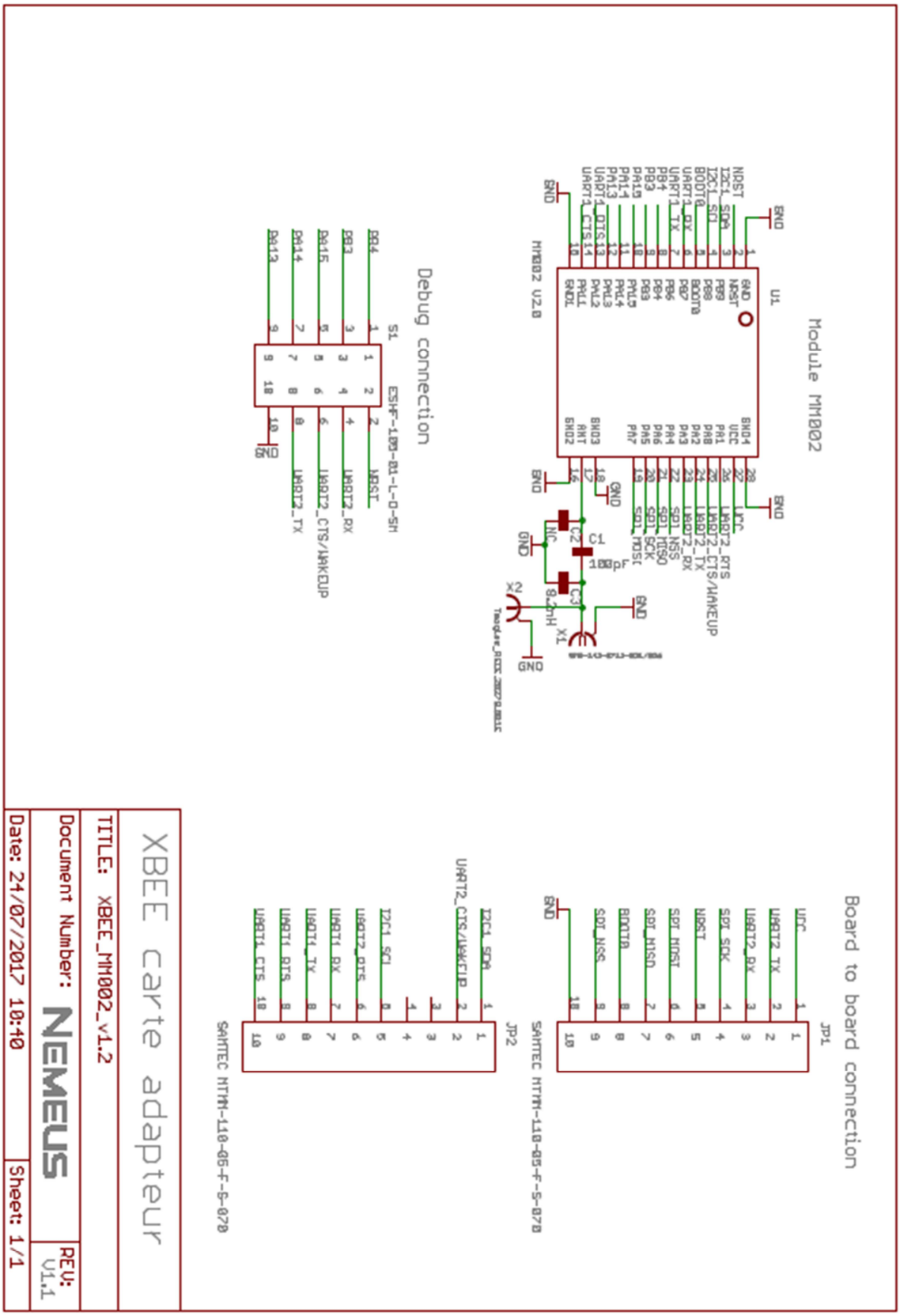
Wiring

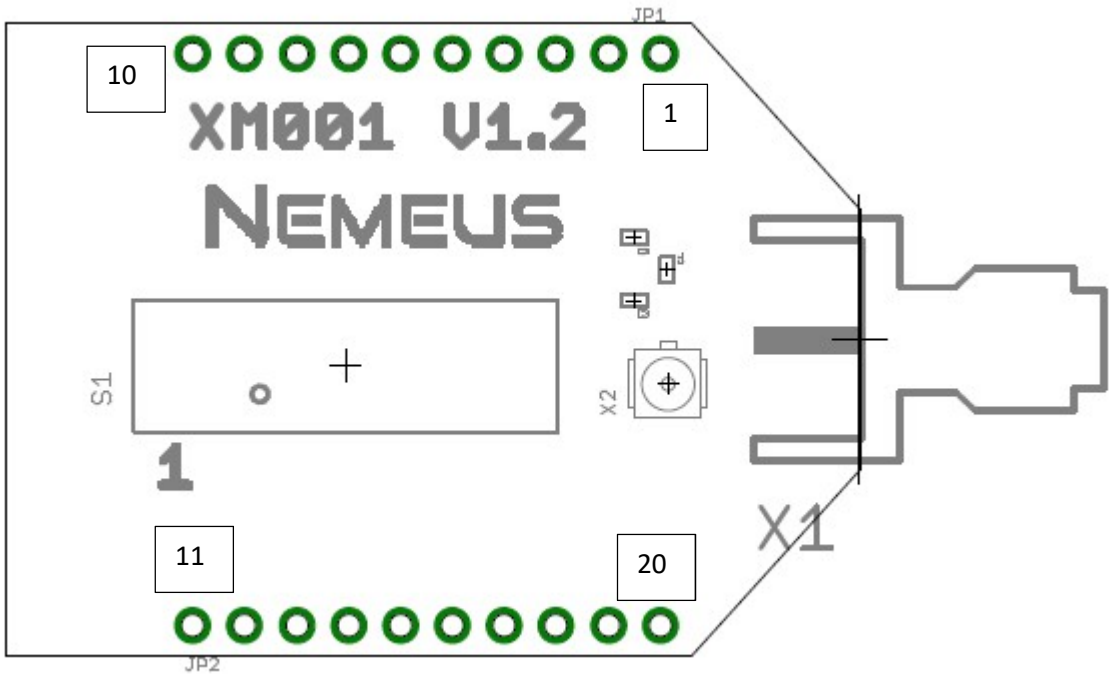
Connector pin number	XBEE signal	Type	Module signal
1	VCC	-	VCC - Power supply
2	DOUT	Output	UART2_TX
3	DIN / nCONFIG	Input	UART2_RX
4	DO8* Output Digital Output 8	Output	SPI_CLK
5	**nRESET**	Input	Module Reset (reset pulse must be at least 200 ns)
6	PWM0 / RSSI	Output	SPI_MOSI
7	PWM1	Output	SPI_MISO
8	[reserved]	-	BOOT0
9	**nDTR**/ SLEEP_RQ / DI8	Input	SPI_NSS
10	GND	-	Ground
11	AD4 / DIO4	Either	I2C_SDA
12	**nCTS**/DIO7	Either	UART2_CTS/ Wakeup
13	ON/**nSLEEP**	Output	NC
14	VREF	Input	NC
15	Associate / AD5 / DIO5	Either	I2C_CLK
16	**nRTS**/AD6/DIO6	Either	UART2_RTS
17	AD4 / DIO4	Either	UART1_RX
18	AD2 / DIO2	Either	UART1_TX
19	AD1 / DIO1	Either	UART1_RTS
20	AD0 / DIO0	Either	UART1_CTS

HW architecture

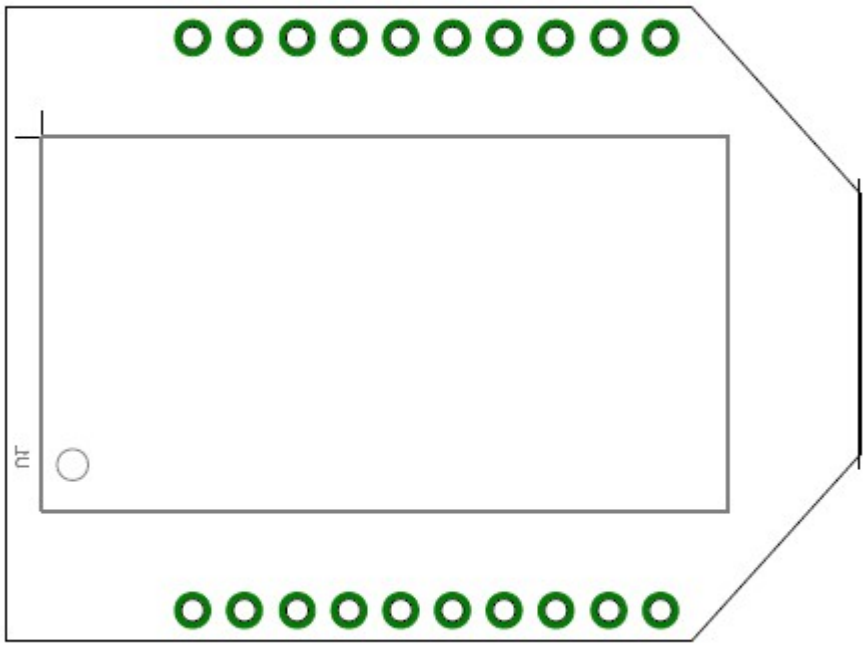


Schematics and placement

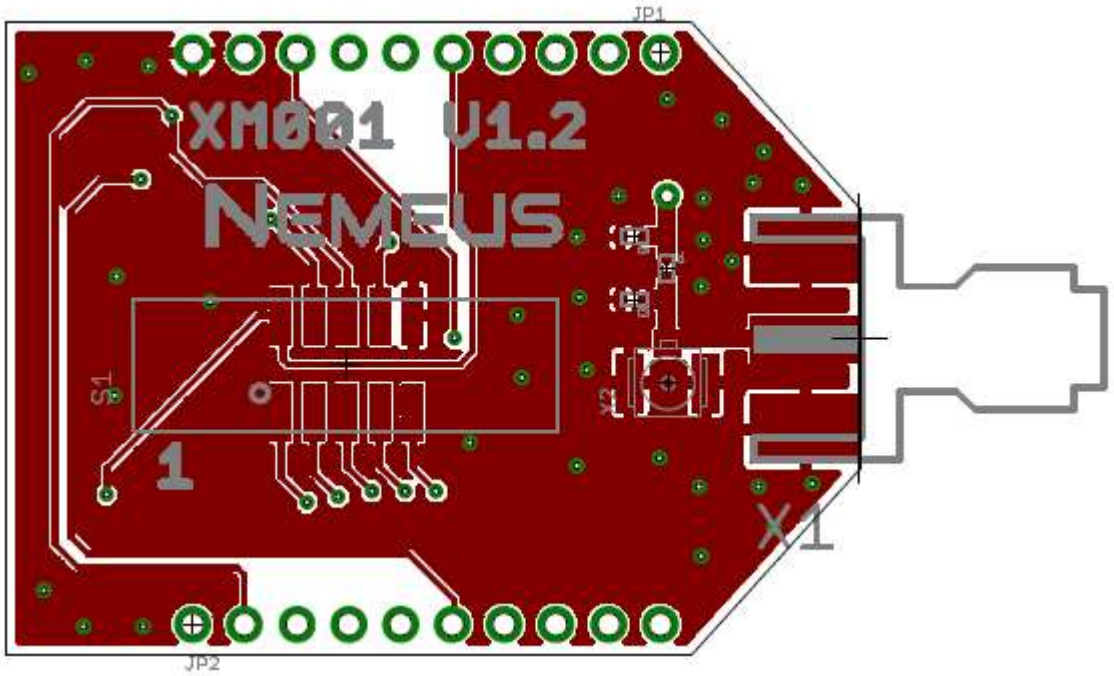




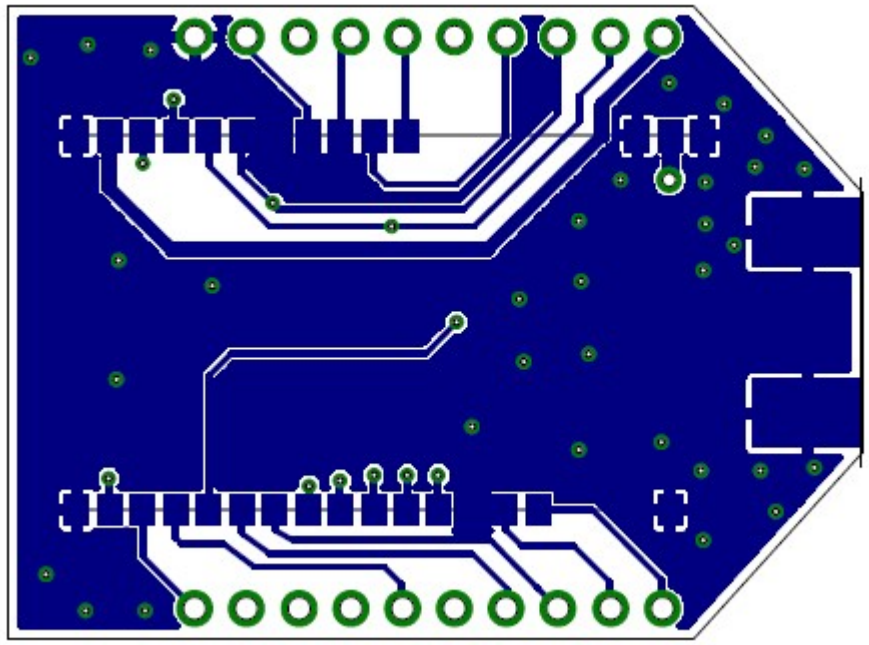
TOP placement



Bottom placement



PCB TOP view



PCB bottom view